

- ◇Structure                               Silicon monolithic integrated circuit
- ◇Product Series                        Lens control LSI
- ◇Type                                     BU24026GU
- ◇Applications                         Digital still cameras
- ◇Functions                             •Waveforming circuit (3 channels)  
   •PI driving circuit (2 channels)  
   •Driver block (1-6 channels)       : Constant voltage control type H-bridge  
   •Driver block (7 channel)         : Constant current control type H-bridge

◇Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	Remark
Power supply voltage	DVDD	-0.3~4.5	V	
	MVCC	-0.3~7.0	V	
	VDDAMP	-0.3~7.0	V	
Input voltage	VIN	-0.3~DVDD+0.3	V	
Input/output current	IIN	±500	mA	Driver block (by MVCC pin)
		+100	mA	by PIOUT pin
Storage temperature range	TSTG	-55~125	°C	
Operating temperature range	TOPE	-20~85	°C	
Permissible dissipation	PD	1.37	W	*1

This product is not designed for anti-radiation applications.

\*1To use at a temperature higher than Ta=25°C, derate 13.7mW per 1°C.

(At mounting 50 mm × 58 mm × 1.75mm glass epoxy board. )

◇Operating conditions(Ta = 25°C)

Parameter	Symbol	Limits	Unit	Remark
Digital power supply voltage	DVDD	2.7~3.6	V	DVDD ≤ MVCC
Driver power supply voltage	MVCC	2.7~5.5	V	
Constant current control amplifier power supply voltage	VDDAMP	2.7~5.5	V	
clock operating frequency	FCLK	1~27.5	MHz	Reference clock

## ◇Electrical characteristics

(Unless otherwise specified, Ta=25°C, DVDD=3.0V, MVCC=5.0V, VDDAMP=5.0V, DVSS=MGND=0.0V)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MIN.		
<Current consumption>						
Quiescence (DVDD)	ISSD	–	30	100	μA	CMD_RS=0
	(MVCC) ISSVM	–	0	5	μA	CMD_RS=0
Operation (DVDD)	IDDD	–	8.5	15.0	mA	CMD_RS=1
<Logic block>						
Low-level input voltage	VIL	DVSS	–	0.3DVDD	V	
High-level input voltage	VIH	0.7DVDD	–	DVDD	V	
Low-level input current	IIL	0	–	10	μA	VIL = DVSS
High-level input current	IIH	0	–	10	μA	VIH = DVDD
Low-level output voltage	VOL	DVSS	–	0.2DVDD	V	IOL = 1.0mA
High-level output voltage	VOH	0.8DVDD	–	DVDD	V	IOH = 1.0mA
<PI driving circuit>						
Output voltage	PIVO	–	0.28	0.50	V	IIH = 50mA
<Waveforming circuit 1ch>						
Detective voltage range	V <sub>th</sub>	0.5	–	2.5	V	SI1
Detective voltage error	V	1/2DVDD – 0.1	1/2DVDD	1/2DVDD + 0.1	V	Waveforming Vth = 20h setting
<Waveforming circuit 2,3ch>						
High-level threshold voltage	V <sub>thH1</sub>	–	–	1.9	V	SI2, SI3 (DVDD=3.25V), Hys ON
Low-level threshold voltage	V <sub>thL1</sub>	0.6	–	–	V	SI2, SI3 (DVDD=3.25V), Hys ON
Hysteresis width	HYS	0.2	–	0.6	V	SI2, SI3 (DVDD=3.25V), Hys ON
threshold voltage	V <sub>thH2</sub>	1.0	–	1.85	V	SI2, SI3 (DVDD=3.25V), Hys OFF
<Constant voltage driver block>						
ON-resistance	R <sub>on</sub>	–	1.5	2.0	Ω	IO = ±100mA
OFF-leak current	IOZ	–10	0	10	μA	Output Hiz setting
Turn-ON time	t <sub>ON</sub>	–	0.15	1.0	μS	
Turn-OFF time	t <sub>OFF</sub>	–	0.1	0.5	μS	
Average voltage accuracy	V <sub>diff</sub>	–5	–	+5	%	V <sub>diff</sub> = 2.0V setting.
<Constant current driver block>						
ON-resistance	R <sub>on</sub>	–	0.9	1.5	Ω	IO = ±100mA
OFF-leak current	IOZ	–10	0	10	μA	Output Hiz setting
Output voltage	VO	188	200	212	mV	DAC setting: 1010.0111, RRNF=1[Ω]
Turn-ON time	t <sub>ON</sub>	–	0.15	1.0	μS	
Turn-OFF time	t <sub>OFF</sub>	–	0.1	0.5	μS	

◇3-wire serial interface

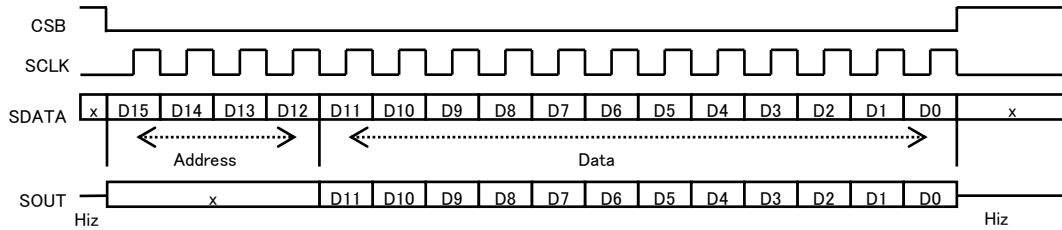
Control commands are framed by 16-bit serial input (MSB first) and input through the CSB, SCLK, and SDATA pins.

4 higher-order bits specify addresses, while the remaining 12 bits specify data.

Data of every bit is input through the SDATA pin, retrieved on the rising edges of SCLK.

Data becomes valid in the CSB Low area. The loading timing is different in the resistor. (as shown in “Note 5,6”)

Furthermore, the interface will be synchronized with the falling edges of SCLK to output the SOUT data of the 12 bits.



<Register map>

Address[3:0]				Data[11:0]												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	ModeA[1:0]		SelA[1:0]		0	Ach different output voltage[6:0]							
0	0	0	1	0	0	0	0	Ach Cycle[7:0]								
				0	0	1	0	Ach Cycle[15:8]								
				1	1	1	0	0	0	APOS[1:0]	0	0	0	0	ASTOP	
0	0	1	0	EnA	RtA	Ach Pulse[9:0]										
0	0	1	1	Ach status[1:0]		Ach operation pulse number[9:0]										
0	1	0	0	ModeB[1:0]		SelB[1:0]		0	Bch different output voltage [6:0]							
0	1	0	1	0	0	0	0	Bch Cycle[7:0]								
				0	0	1	0	Bch Cycle[15:8]								
				1	1	1	0	0	0	BPOS[1:0]	0	0	0	BSTOP		
0	1	1	0	EnB	RtB	Bch Pulse[9:0]										
0	1	1	1	Bch status[1:0]		Bch operation pulse number[9:0]										
1	0	0	0	ModeC[1:0]		SelC[1:0]		0	Cch different output voltage [6:0]							
1	0	0	1	0	0	0	0	Cch Cycle[7:0]								
				0	0	1	0	Cch Cycle[15:8]								
				1	0	1	5_PWM_Ct[1:0]		5ch different output voltage[6:0]							
				1	1	0	6_PWM_Ct[1:0]		6ch different output voltage[6:0]							
				1	1	1	0	0	0	CPOS[1:0]	0	0	0	CSTOP		
1	0	1	0	EnC	RtC	Cch Pulse[9:0]										
1	0	1	1	Cch status[1:0]		Cch operation pulse number[9:0]										
1	1	0	0	0	0	Chopping[1:0]	CacheM	SEL56[2:0]		P_CTRL	CLK_DIV[2:0]					
1	1	0	1	0	0	0	0	0	0	0	0	0	0	PI_CTRL1	PI_CTRL2	
				0	0	1	0	0	5_PULSE_CNT	5_PULSE_BASE[1:0]	0	6_PULSE_CNT	6_PULSE_BASE[1:0]			
				0	1	0	0	5_PULSE_COUNT[7:0]								
				0	1	0	1	6_PULSE_COUNT[7:0]								
				0	1	1	0	0	EXT_EN	0	EXT_RT	EXT_NUM[3:0]				
				1	0	0	0	EXT_PAT1							EXT_PAT0	
				1	0	0	1	EXT_PAT3							EXT_PAT2	
				1	0	1	0	EXT_PAT5							EXT_PAT4	
				1	0	1	1	EXT_PAT7							EXT_PAT6	
				1	1	0	0	EXT_PAT9							EXT_PAT8	
				1	1	1	0	EXT_PAT11							EXT_PAT10	
1	1	1	1	EXT_PAT13							EXT_PAT12					
1	1	1	1	EXT_PAT15							EXT_PAT14					
1	1	1	0	0	0	0	0	Constant current driver reference voltage adjustment 8bit DAC[7:0]								
				0	1	0	0	0	0	0	0	0	0	7_CTRL[1:0]		
				1	0	0	0	0	0	Wavfoming circuit 1 Vthh[5:0]						
				1	0	0	1	0	0	Wavfoming circuit 1 Vthl[5:0]						
				1	0	1	0	0	0	0	0	0	0	HYS3	HYS2	
1	1	0	0	0	0	0	0	0	0	0	0	CMD_RS				
Addresses other than those above				Setting prohibited												

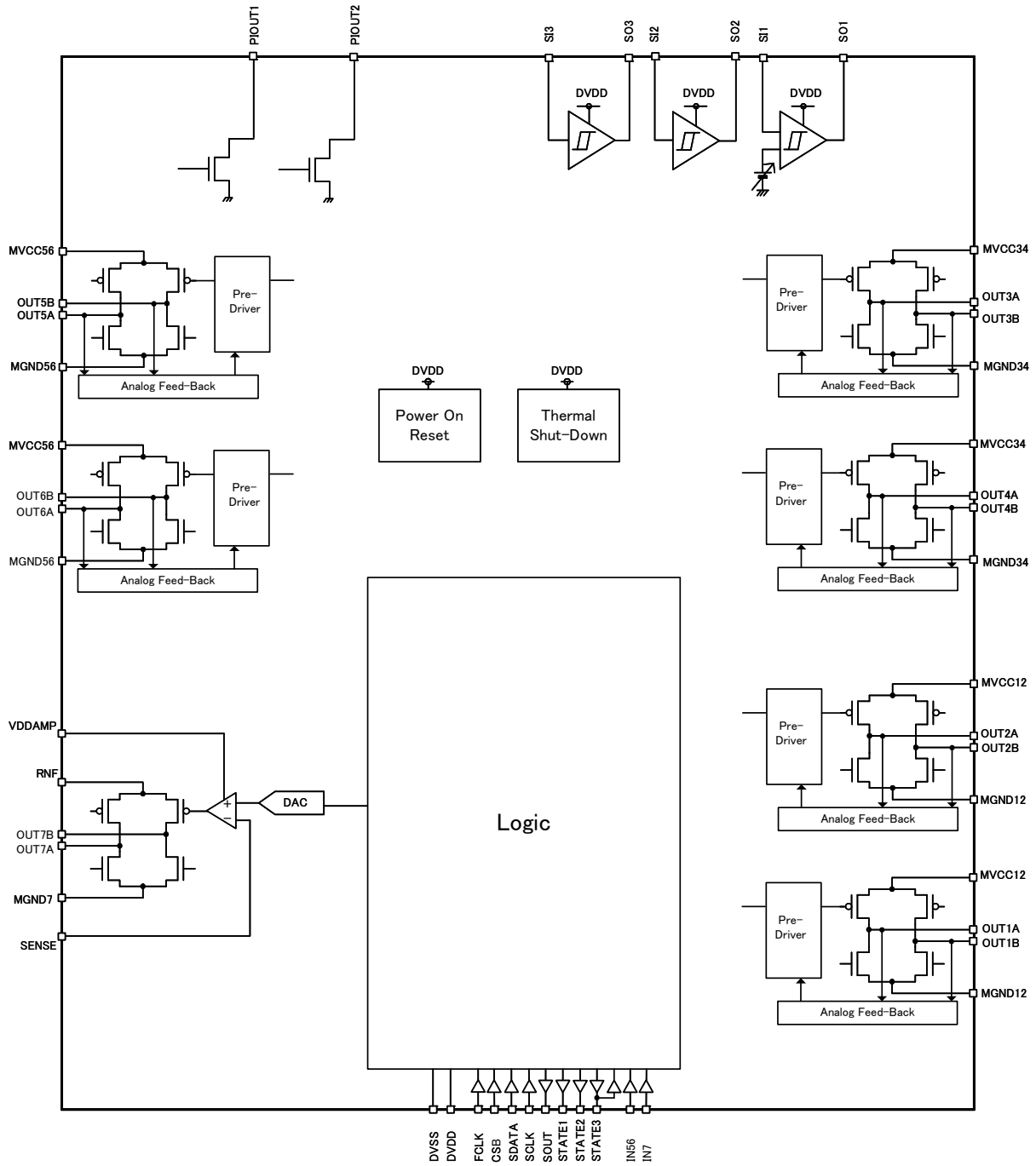
(Note 1) The notations A, B, C in the register map correspond to Ach, Bch and Cch respectively.

(Note 2) The Ach is defined as 1ch and 2ch driver output, the Bch as 3ch and 4ch driver output, and Cch as 5ch and 6ch driver output.

(Note 3) After resetting (Power ON reset, and CMD\_RS), “initial setting” is saved in all registers.

- (Note 4) The addresses 4' b0011, 4' b0111, and 4' b1011 have data (status[1:0], operation pulse number[9:0]), which are internal register values and output from the SOUT pin.
- (Note 5) For Mode, different output voltage, Cycle, En, and Rt registers, data that are written before the access to the Pulse register becomes valid, and determined at the rising edge of CSB after the access to the Pulse register. (The Mode, different output voltage, Cycle, En, Rt, and Pulse registers contain Cache registers, but any registers other than those do not contain with such registers.)
- (Note 6) For POS, STOP, PWM\_Ct, and different output voltage registers, data are determined at the rising edge of CSB, and for any registers other than those, data are determined at the rising edge of 16th SCLK.

◇Block Diagram



◇Pin functions

Land	Pin name	Power	Function	I/O	Handling of unused pins
E6	DVDD	-	Digital power supply	Power supply	-
E2	DVSS	-	Ground	GND	-
C2	FCLK	DVDD	main clock logic input	I	pull down(DVSS)
D4	CSB	DVDD	Serial control chip select input	I	pull up(DVDD)
B3	SCLK	DVDD	Serial control clock input	I	pull down(DVSS)
D3	SDATA	DVDD	Serial control data input	I	pull down(DVSS)
B5	SOUT	DVDD	Serial control data output	O	open
E4	STATE1	DVDD	STATE1 1,2ch condition logic output	O	open
F4	STATE2	DVDD	STATE2 3,4ch condition logic output	O	open
F5	STATE3	DVDD	STATE 3 5,6ch condition logic output / 5,6ch control logic input	I/O(initial condition: O)	open
D5	IN56	DVDD	5,6ch control logic input	I	pull down(DVSS)
C5	IN7	DVDD	7ch control logic input	I	pull down(DVSS)
E3	PIOUT1	DVDD	PI driving output1	O	open
D2	PIOUT2	DVDD	PI driving output2	O	open
E5	SI1	DVDD	1ch waveforming input(With adjustment function of threshold voltage)	I	pull down(DVSS)
B4	SI2	DVDD	2ch waveforming input	I	pull down(DVSS)
C6	SI3	DVDD	3ch waveforming input	I	pull down(DVSS)
F3	SO1	DVDD	1ch waveforming output	O	open
C4	SO2	DVDD	2ch waveforming output	O	open
D6	SO3	DVDD	3ch waveforming output	O	open
A1, B2※	MVCC12	-	1-2channel driver power supply	Power supply	-
A4	MGND12	-	1-2channel driver ground	GND	-
A2	OUT1A	MVCC12	1-channel driver A output	O	open
A3	OUT1B	MVCC12	1-channel driver B output	O	open
A5	OUT2A	MVCC12	2-channel driver A output	O	open
A6	OUT2B	MVCC12	2-channel driver B output	O	open
A7, B6※	MVCC34	-	3-4channel driver power supply	Power supply	-
D7	MGND34	-	3-4channel driver ground	GND	-
B7	OUT3A	MVCC34	3-channel driver A output	O	open
C7	OUT3B	MVCC34	3-channel driver B output	O	open
E7	OUT4A	MVCC34	4-channel driver A output	O	open
F7	OUT4B	MVCC34	4-channel driver B output	O	open
G5	MVCC56	-	5-6channel driver power supply	Power supply	-
G3	MGND56	-	5-6channel driver ground	GND	-
G6	OUT5A	MVCC56	5-channel driver A output	O	open
F6, G7※	OUT5B	MVCC56	5-channel driver B output	O	open
G4	OUT6A	MVCC56	6-channel driver A output	O	open
G2	OUT6B	MVCC56	6-channel driver B output	O	open
D1	RNF	-	7-channel driver power supply	Power supply	-
B1	MGND7	-	7-channel driver ground	GND	-
F2, G1※	VDDAMP	-	Power supply of constant current driver control	Power supply	-
F1	SENSE	VDDAMP	Negative input for constant current driver control	I	pull down(MGND7)
E1	OUT7A	RNF	7-channel driver A output	O	open
C1	OUT7B	RNF	7-channel driver B output	O	open
C3	INDEX	-	Index pin	-	-

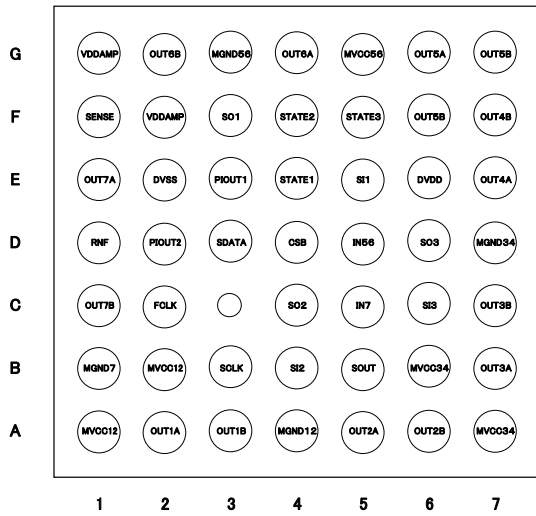
※It is not possible to use corner pin only. (Corner pins are A1, A7, G1, and G7.)

Please use A1-B2, A7-B6, F2-G1, F6-G7 pair respectively or using B2, B6, F2, F6 only.

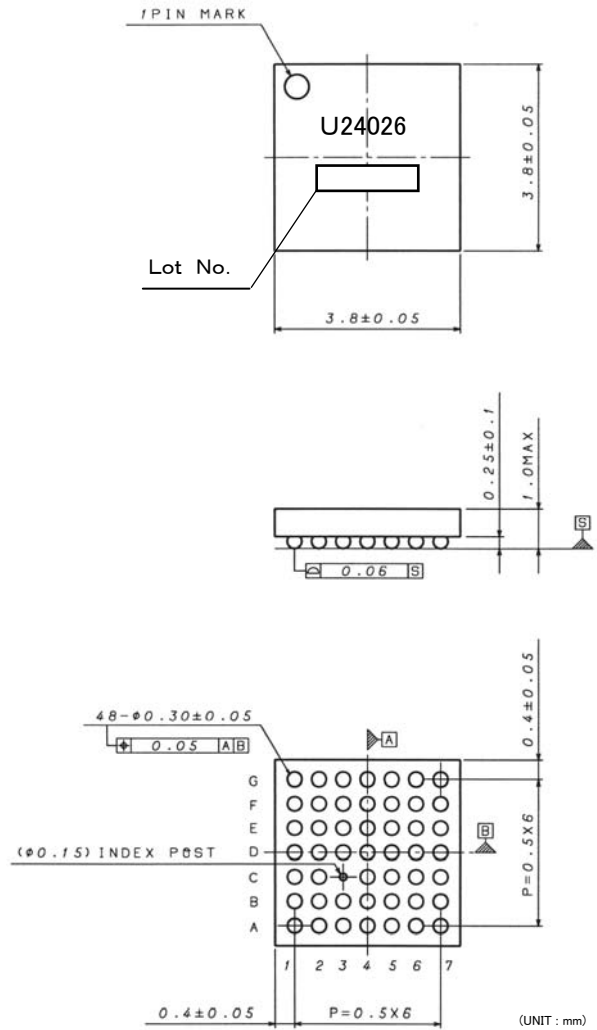
◇ Pin related equivalent circuit diagrams

Pin	Equivalent circuit diagram	Pin	Equivalent circuit diagram
FCLK, CSB, SCLK SDATA, IN56, IN7, SI2, SI3  *SI2,SI3 are the Schmitt inputs.		SENSE	
SOUT, STATE1, STATE2, SO1, SO2, SO3		PIOUT1, PIOUT2	
OUT1A, OUT1B, OUT2A, OUT2B		OUT3A, OUT3B, OUT4A, OUT4B	
OUT5A, OUT5B OUT6A, OUT6B		OUT7A, OUT7B RNF	
STATE3		SI1	

◇Pin assignment diagram (reverse side)



◇Outline dimensions/Marking figure



VCSP85H3

◇Cautions on use

- (1) Absolute maximum ratings  
If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you expect that any voltage or temperature could be exceeding the absolute maximum ratings, take physical safety measures such as fuses to prevent any conditions exceeding the absolute maximum ratings from being applied to the LSI.
- (2) GND potential  
Maintain the GND pin at the minimum voltage even under any operating conditions.  
Actually check to be sure that none of the pins have voltage lower than that of GND pin, including transient phenomena.
- (3) Thermal design  
With consideration given to the permissible dissipation under actual use conditions, perform thermal design so that adequate margins will be provided.
- (4) Short circuit between pins and malfunctions  
To mount the LSI on a board, pay utmost attention to the orientation and displacement of the LSI. Faulty mounting to apply a voltage to the LSI may cause damage to the LSI. Furthermore, the LSI may also be damaged if any foreign matters enter between pins, between pin and power supply, or between pin and GND of the LSI.
- (5) Operation in strong magnetic field  
Make a thorough evaluation on use of the LSI in a strong magnetic field. Not doing so may malfunction the LSI.

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